AMENDMENTS TO THE CLAIMS

1. (currently amended): A memory cell, comprising:

a substrate, said substrate including a source region and a drain region;

a first insulating layer over said substrate;

a first conductive layer over said first insulating layer[[;]] and between said source and drain regions;

a programmable conductance element over said first conductive layer, ~~electrode,~~ said programmable conductance element having a resistance which is controllable between at least two states; and

a second conductive layer over said programmable conductance element.

2. (original): The memory cell of claim 1, wherein said programmable conductance element is comprised of a chalcogenide glass.

3. (original): The memory cell of claim 2, wherein said chacogenide glass is comprised of germanium-selenide.

4. (original): The memory cell of claim 2, wherein said chacogenide glass comprises Ge_xSe_{100-x}.

5. (original): The memory cell of claim 4, wherein x has a range of from 18 to 43.

6. (original): The memory cell of claim 5, wherein x is 20.

7. (original): The memory cell of claim 2, wherein said chacogenide glass is doped with a metal.

8. (original): The memory cell of claim 2, wherein said chacogenide glass is doped with silver.

9. (original): The memory cell of claim 1, wherein said first and second conductive layers are comprised of one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

10 – 25. (canceled):

26. (currently amended): A memory device, comprising:

a control circuit;

a memory array, coupled to said control circuit, said memory array further comprising a plurality of blocks, each of said plurality of blocks including a plurality of memory cells,

wherein each of said memory cells comprises,

a substrate, the substrate having a source region and a drain region;

a first insulating layer over said substrate;

a first conductive layer over said first insulating layer[[;]] and between said source and drain regions;

a programmable conductance element over said first conductive layer, ~~electrode,~~ said programmable conductance element having a resistance which is controllable between two states; and

a second conducive layer over said programmable conductance element.

27. (original): The device of claim 26, wherein said programmable conductance element is comprised of a chalcogenide glass.

28. (original): The device of claim 27, wherein said chacogenide glass is comprised of germanium-selenide.

29. (original): The device of claim 27, wherein said chacogenide glass is comprised of Ge_xSe_{100-x}.

30. (original): The device of claim 29, wherein x has a range of 18 to 43.

31. (original): The device of claim 30, wherein x is 20.

32. (original): The device of claim 26, wherein said chacogenide glass is doped with a metal.

33. (original): The device of claim 26, wherein said chacogenide glass is doped with silver.

34. (original): The device of claim 26, wherein said first and second conductive layers are comprised of one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

35. (currently amended): A processor based system, comprising:

a processor;

a memory device, said memory device including a plurality of memory cells,

wherein each of said memory cells comprises,

a substrate, the substrate having a source region and a drain region;

a first insulating layer over said substrate;

a first conductive layer over said first insulating layer[[;]] and between said source and drain regions;

a programmable conductance element over said first conductive layer, ~~electrode,~~ said programmable conductance element having a resistance which is controllable between two states; and

a second conductive layer over said programmable conductance element.

36. (original): The device of claim 35, wherein said programmable conductance element is comprised of a chalcogenide glass.

37. (original): The device of claim 36, wherein said chacogenide glass is comprised of germanium-selenide.

38. (original): The device of claim 36, wherein said chacogenide glass has a chemical formula of Ge_xSe_{100-x}.

39. (original): The device of claim 38, wherein x has a range of 18 to 43.

40. (original): The device of claim 39, wherein x is 20.

41. (original): The device of claim 36, wherein said chacogenide glass is doped with a metal.

42. (original): The device of claim 36, wherein said chacogenide glass is doped with silver.

43. (original): The device of claim 35, wherein said first and second conductive layers are comprised of one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

44. (currently amended): The memory cell of claim 1, wherein said programmable conductance element is a multi-layer structure comprised of:

a first layer comprising $Ge_{40}Se_{60}$;

a second layer, formed over said first layer, said second layer comprising,

at least one of,

a sublayer of Ag, and

a sublayer of Ag_2Se;

a third layer, formed over said second layer, comprised of $Ge_{40}Se_{60}$;

a fourth layer, formed over said third ~~second~~ layer, comprising Ag; and

a fifth layer, formed over said fourth layer, comprising $Ge_{40}Se_{60}$.

45. (currently amended): The memory cell of claim 26, wherein said programmable conductance element is a multi-layer structure comprised of:

a first layer comprising $Ge_{40}Se_{60}$;

a second layer, formed over said first layer, said second layer comprising,

at least one of,

a sublayer of Ag, and

a sublayer of Ag_2Se;

a third layer, formed over said second layer, comprised of $Ge_{40}Se_{60}$;

a fourth layer, formed over said third ~~second~~ layer, comprising Ag; and

a fifth layer, formed over said fourth layer, comprising $Ge_{40}Se_{60}$.

46. (currently amended): The system of claim 35, wherein said programmable conductance element is a multi-layer structure comprised of:

a first layer comprising $Ge_{40}Se_{60}$;

a second layer, formed over said first layer, said second layer comprising,

at least one of,

a sublayer of Ag, and

a sublayer of Ag_2Se;

a third layer, formed of said second layer, comprised of $Ge_{40}Se_{60}$;

a fourth layer, formed over said third ~~second~~ layer, comprising Ag; and

a fifth layer, formed over said fourth layer, comprising $Ge_{40}Se_{60}$.